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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,899	04/16/2004	Syun-Ming Jang	24061.231/TSMC2003-1383	2231

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EXAMINER	
LOUIE, WAI SING	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,899	JANG ET AL.	
	Examiner	Art Unit	
	Wai-Sing Louie	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *35-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of Group I, claims 1-34, in the reply filed on 3/1/05 is acknowledge. The invention in Group I is a semiconductor device comprises a logic device and a memory device on the same substrate and the invention in Group II is a method of manufacturing the device. Group I and Group II are related as process of making and product made. Therefore, the inventions are distinct and the restriction is proper. The restriction is final. It is suggested that non-elected claims 35-40 be canceled in the response to this Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 8-9, 12, 14-17, 20-24, 27-28, 30-31 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Montree et al. (US 6,251,729).

With regard to claims 1, 17, Montree et al. disclose a memory device (col. 6, line 3 to col. 9, line 11 and fig. 10), comprising:

- a substrate 1 (col. 6, line 11 and fig. 10);

- a logic device (MOS transistor) formed over the substrate 1 (col. 6, lines 3-4 and fig. 10), where the logic device comprises a high dielectric constant gate dielectric 23 (col. 7, lines 39-47 and fig. 10);
- a memory device (non-volatile memory) formed over the substrate 1 (col. 6, line 4 and fig. 10), where the memory device comprises a non-high-k gate dielectric 13 (col. 6, lines 22-23 and lines 46-47);
- a gate electrode 11 over the non-high-k gate dielectric 13 (fig. 10).

With regard to claims 3-4, 12, 14-15, 20, and 30, Montree et al. disclose the high-k gate dielectric is in the range from 7 to 25 (col. 5, lines 1-6) using the materials such as Ta_2O_5 and Al_2O_3 and Si_3N_4 (col. col. 7, lines 44-47).

With regard to claim 5, Montree et al. disclose the logic device is a metal-oxide semiconductor (MOS) field-effect transistor (col. 6, lines 3-4).

With regard to claims 8-9 and 27-28, Montree et al. disclose the memory device comprises a non-volatile memory such as EEPROM or EPROM (col. 6, lines 3-10).

With regard to claims 16, 21, Montree et al. disclose the non-high-k gate dielectric is silicon oxide (col. 6, lines 22-23).

With regard to claims 22-24, Montree et al. disclose the substrate 1 is an insulated silicon substrate (col. 6, lines 11-16 and fig. 1).

With regard to claim 31, Montree et al. disclose the logic gate electrode comprises titanium nitride (col. 8, lines 23-27).

With regard to claim 33, Montree et al. disclose the gate electrode comprises polysilicon (col. 8, lines 18-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montree et al. (US 6,251,729) in view of Bruley et al. (US 6,884,641).

With regard to claim 2, Montree et al. do not disclose the substrate comprises defective crystalline to accommodate logic devices with strained channel. However, Bruley et al. disclose the source/drain junction of the MOSFET is strained and the defect is localized in the channel area (Bruley col. 4, lines 22-27). Bruley et al. teach able to detect the defect in the shallow junction enables the layout of the junction depth and the effective implantation of the source/drain (Bruley col. 4, lines 35-42). Montree et al. and Bruley et al. have substantially the same environment of an integrated circuit device having a MOSFET device. Therefore, it would have been obvious for the one with ordinary skill in the art to modify Montree's device with the teaching of Bruley et al. to have defective crystalline in the strained channel in order to layout of the junction depth and the effectively implant of the source/drain.

With regard to claim 7, Montree et al. modified by Bruley et al. would disclose a SRAM memory device in the semiconductor IC device (Bruley col. 4, line 38).

Claims 6 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montree et al. (US 6,251,729) in view of Liu et al. (US 6,066,525).

With regard to claims 6 and 25-26, Montree et al. do not disclose the memory device is a dynamic random access memory (DRAM). However, Liu et al. disclose an integrated circuit (IC) chip comprises two DRAM cells (Liu col. 4, line 43-45). Liu et al. disclose the DRAM cells allows large capacity of memory storage (Liu col. 1, lines 30-35). Montree et al. and Liu et al. have substantially the same environment of semiconductor IC device having a logic device and memory device. Therefore, it would have been obvious for the one with ordinary skill in the art to modify Montree's device with the teaching of Liu et al. to include a DRAM in the memory device in order to have a large capacity of memory storage. Montree et al. modified by Liu et al. do not disclose a trench-type DRAM device. However, the stack-type and trench-type DRAM are function the same. Therefore, the changes in shape of the product are held to have been obvious for a person of ordinary skill in the art. In re Daily 149 USPQ 47, 50 (CCPA 1966). See also Glue Co. v. Upton 97 US 3, 24 (USSC 1878).

Claims 10-11, 32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montree et al. (US 6,251,729).

With regard to claims 10-11, 32, and 34, Montree et al. disclose the thickness of the high-k gate dielectric is 6-10 nm and the low-k gate dielectric is less than 1.5-4 nm, but do not disclose the thickness of the high-k gate dielectric is less than 5 nm; the low-k gate dielectric is less than 1.5 nm; and the gate electrode thickness. Since the applicant has not established the

criticality of the thicknesses stated and since these thicknesses are in common use in similar devices in the art, it would have been obvious to one of ordinary skill in the art to use these values in the device. Where patentability is said to be based upon particular chosen dimension or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 13 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montree et al. (US 6,251,729) in view of Nakajima (US 6,787,863).

With regard to claims 13, 19, Montree et al. disclose using high-k gate dielectric constant material for the MOSFET device, but do not list hafnium oxide as one of the material. However, Nakajima discloses using hafnium oxide as gate insulating film 20 (Nakajima col. 3, lines 26-30). Nakajima teaches high dielectric constant material inhibiting leakage current (Nakajima col. 3, lines 30-34). Montree et al. and Nakajima have substantially the same environment of MOSFET having high-k gate dielectric insulating film. Thus, it would have been obvious at the time the invention was made to modify Montree's device with the teaching of Nakajima using hafnium oxide as high-k gate dielectric insulating film in order to inhibiting leakage current.

With regard to claim 18, Montree et al. modified by Nakajima would disclose a silicon nitride insulating layer under the high-k gate dielectric film 20 (Nakajima fig. 1).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Montree et al. (US 6,251,729) in view of Nowak et al. (US 6,794,718).

With regard to claim 29, Montree et al. do not disclose the MOSFET comprises a channel in <100> crystalline direction. However, Nowak et al. disclose the channel region of the FET is form along the <100> plane of the SOI wafer (Nowak col. 4, lines 41-44). Nowak et al. teach the electrons have their greatest mobility in <100> plane (Nowak col. 1, lines 39-41). Montree et al. and Nowak et al. have substantially the same environment of semiconductor IC device having a MOSFET device on the SOI substrate. Thus, it would have been obvious at the time the invention was made to modify Montree's device with the teaching of Nowak et al. to form the MOSFET in the <100> crystalline direction in order to have a high mobility device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wsl
May 5, 2005.